During the last months we conducted a poll about what you guys would you like to read more about on ThinkVerification and here are the results:

Verification Methodology - 41%

SystemVerilog Tutorials - 31%

e Tutorials - 13%

Interviews - 12%

Lightweight Articles - 4%

Looks like most of you would like to learn more about advanced verification methodology, especially with SystemVerilog. That's a very clear message. We'll try to focus on that area in the coming months, and in the meantime we'd appreciate it if you could send us more specific requests (as some of you already have). You can also leave them as comments if you like.

In the meantime, if you haven't already seen our VMM Hackers Guide series , you might find it interesting.

And on that note - did you like our autodup utility? if you did, please drop us a line or leave a comment to encourage us to develop more stuff for you!

Oh, and have we ever mentioned how important t your feedback is to us?

Seriously, even if you're not into the whole commenting thing please just devote 5 seconds of your time to take the poll (at the upper right of this page) to tell us what you think.

Happy Verifying!