SystemVerilog emerged a few years ago and has gained phenomenal popularity ever since. Today this language is virtually ubiquitous and all 3 big EDA vendors keep pushing it forward. So if you consider yourself a modern verifier, you'd better get familiar with SystemVerilog unless you want to stay in the dark.

While Think Verification focuses on the advanced stuff (check out our VMM Hacker's Guide series), there are many websites and blogs out there that offer free tutorials that can help you learn the basics of SystemVerilog. Here are a few links that will help you get started very quickly:

ASIC WORLD

A comprehensive tutorial that shows you most of the constructs and elements of the language. There's far more information than you need to get you through your first steps, but it's a good place to keep as reference. The examples given there also include snapshots from the simulator's output which is cool. Methodology is not covered there, although the author intends to cover that in the future.

DOULOS

Probably the first place to look. Doulos offers a sleek tutorial covering some of the most important elements of SystemVerilog in a nutshell. Although not comprehensive, we think their tutorial gives a nice overview of the language fundamentals that you should get familiar with, especially if you have experience in other HVLs. Their quick tutorial on Classes and Randomization will get you started rapidly.

ELECTRO-SOFTS

This tutorial covers the basic constructs of SystemVerilog quite thoroughly, along with some good examples. This might be a good place to go once you nail the basic concepts of the language. Methodology is not covered here but we liked their SVA (System Verilog Assertions) section.

TESTBENCH.IN

A comprehensive tutorial that covers all of SystemVerilog's fundamentals, including OOP and DPI. They also cover VMM quite well. There are a couple of labs for you to download if you're up for it. Overall - a great tutorial that teaches language as well as methodology.

SPECMAN-VERIFICATION

An evolving (and funny) tutorial on SystemVerilog that's quite different from the other "serious" looking tutorials out there. Avidan (the author) shares with us not only the basic constructs of SV but also his philosophical view on each one of them. Definitely worth a visit if you're into learning SystemVerilog.

The 3 M's of Verification: Methodology! Methodology! Methodology!

SystemVerilog alone is not enough if you're serious about building verification environments. That's where standard methodology comes in. Today there are two main methodologies in the market for SystemVerilog. The first is VMM, the other is OVM. Both methodologies can do the job and there's plenty of information out there on each one of them. OVM-World and VMM-Central are probably the best places to start looking (pretty soon a new methodology is going to conquer the world - UVM, which is based on OVM plus parts of VMM). A word of advice - pay as much attention to methodology as you would to language constructs and syntax. In HVLs, and in SystemVerilog in particular, methodology accounts for the greater part of your verification project.