Succeeding at job interviews requires practice. If you're applying for a verification job you'd better get yourself well prepared both mentally and technically. Nevertheless, a great deal of tension could be avoided if you knew in advance what sort of technical questions you might be facing. Different managers will ask different questions, usually from their own area of expertise, and not necessarily yours. So, we've collected for you some of the best websites that offer job interview questions that should help you in your next verification job interview. Wouldn't hurt to review them and plan your answers in advance.

A great source for questions (not many answers though) about SystemVerilog, Verilog, and Specman - http://www.testbench.in/IQ_00_INDEX.html

Applying for a Specman job? Make sure to check this out - http://www.specman-verification.com/index.php?entry=entry061218-182034

Not really verification, but if you're applying for a SystemVerilog job, it's good to know this as well - http://www.rficdesign.com/verilog-interview-question

Practice Perl questions here - http://www.techinterviews.com/perl-interview-questions-and-answers

Tricky riddles, some interviewers like to challenge their candidates... http://www.vlsichipdesign.com/index.php/Chip-Design-Articles/interview-puzzles.html

More tips from us:

- Try to find out what HVL (SystemVerilog, e, SystemC, etc.) you'll be programming in. Practice your programming skills in that language before the interview.
- Practice on presenting your last verification project. You should be able to draw a block diagram and tell what parts were under your responsibility. Know all the details!
- Think of at least 3 big achievements that you were resonsible for in your last project. If your recommenders can reconfirm that later - it's even better.
- Don't be afraid to tell that you LIKE verification and wish to become a professional in that area. Managers don't always realize that.

If you find additional sources please share!