A couple of years ago I wrote here about how the UVM was becoming the next big thing in the verification world.

And guess what? I was right. Not that it was too hard to predict... but anyway, the industry has finally standardized on language (SV) and methodology (UVM) which is great news for us verification folks. The bad news is that even with SystemVerilog and UVM becoming ubiquitious, still we have to spend a fair amount of our time debugging our DUTs. And this is where the tools can be of much help.

Here are some cool tips for using DVE when you're debugging your UVM test bench.

Produced and narrated by yours truly, enjoy !

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See ya!