As the EDA industry seems to be making moves towards a Unified Verification Methodology (OVM + VMM) we thought this would be a great opportunity to share a couple of things that have been on our wish-list for quite a while.

First, we'd like to have an option to set loggers verbosity/severity to Auto. What does Auto mean? Let's say you have a failing test and you want to rerun it with verbosity set to high. Why run twice? What if you could tell the loggers to automatically raise their verbosity levels just before and after a DUT error occurs? (This involves buffering the log file but it's a small price to pay).

Another issue on our wish list has to do with random stability. Sometimes you want to save a test-case and its respective seed number in order to be able to reproduce a specific scenario later on (let's say for regression purposes). But, what happens if the database has evolved by the time you want to reproduce it in such a way that the same seed would generate a different scenario? Well, not sure if it's feasible, but it would definitely be nice to have a function that compares 2 environments in terms or random stability, so we could know if a certain test-case plus seed would produce the same scenario on both of them. Alternatively - maybe we should simply have an option to **un**randomize a test? That means automatically generating a directed test-case from a random test + seed. *[Tip: You can intentionally create a set of directed tests to cover specific points of interest that arise every now and then - read our article about randomization]*

And one final thing - how about adding an option to select a signal or a group or signals on the waveform viewer and autoatically generate the necessary SystemVerilog or ***e*** code (ports, hdl_path, hdl_expression, interface construct, clocking block, etc) to access them?